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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/805,200 | 03/14/2001 | William P. Moore | BU9-98-050DIV1 | 2598 |

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| EXAMINER | |
|---|---|
| GERSTL, SHANE F | |
| **ART UNIT** | **PAPER NUMBER** |
| 2183 | 6 |

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.



3

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/805,200 | MOORE ET AL. | |
| | Examiner | Art Unit | |
| | Shane F Gerstl | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 April 2004 and 05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4,6,9 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,9 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-4, 6, 9, and 20 have been examined.

### *Papers Received*

2. Receipt is acknowledged of both Preliminary Amendments and the Information Disclosure Statement papers submitted, where the papers have been placed of record in the file.

### *Drawings*

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: S41-S52. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Specification*

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Microprocessor Including Microcode Unit for Reduced Power Consumption and Method Therefor that Changes the Value of only those Control Signals Which Must be Changed.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 20 is rejected under 35 U.S.C. 102(b) as being anticipated by Damouny (4,713,750).

7. In regard to claim 20, Damouny discloses a method of providing a state machine decoding, comprising:

a. decoding a current opcode to provide a decode; Column 3, lines 41-49 and column 4, lines 30-35 show that an opcode is mapped or decoded.

b. setting required functions signals; This section also show that the pointers are necessary for execution and thus are required functions signals

c. setting exclusive functions outside of the current opcode to a previous state; Column 18, lines 1-8 show that pointers generated by previous instructions (outside the current opcode) pass through other latches, thus functionally setting theses exclusive DODA and EXEC latches to a previous state (due to the previous instructions)

and latching results of the decode. Column 4, lines 35-38 show that the pointers resulting from the decode are stored in a latch.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-4, 6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Damouny in view of Thoma (4,484,268).

10. In regard to claim 1,

a. Damouny discloses a microprocessor, comprising: a microcode unit (figure 1A, element 54) for outputting control signals (element 182), for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:

i. an instruction address input for receiving an instruction address; Figure 1A shows that element 156 (and thus the microcode unit) receives addresses on an input via line 168, which is output by element 164, for the next microaddress or microinstruction address.

ii. a control variable input for receiving a control variable corresponding to a current state of the microprocessor; Figure 1A shows that the microcode unite has a control variable input 184. Column 4, lines 57-61 show that the input signals received on bus 184 correspond to and control the internal state.

iii. a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; Figure 1A shows that element 180 (and thus the microcode unit) receives on an input the control signal 182, which is output by element 164 and thus the microcode unit. Column 4, lines 57-61 show that this signal 182 is a

control signal. Column 18, lines 1-8 show that the signal on bus 182 is generated in previous instructions and supplied in a next cycle.

iv. An embedded logic circuit dedicated for evaluating one unique type of instruction received by the microcode unit. Figure 1A shows an embedded logic PLA circuit 180 that decodes branch conditions for branch instructions. Column 4, lines 53-61 show that this branch PLA generates the control for selecting the NMA or next microaddress based on branch conditions and thus evaluates branch instructions (a unique type of instruction).

b. Damouny does not disclose a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit.

c. Thoma has disclosed in figure 1 the use of multiple PLA embedded logic circuits. Column 2, lines 6-9 show that each PLA is optimized for decoding a given instruction class (or evaluating a unique instruction type).

d. The background section of Thoma shows that prior art PLA decoding using only one PLA results in physically large design and performance degradation manifest in slower machine speeds. The summary shows that the improvement is in using multiple PLA's and thus this performance degradation is avoided. This ability to have a better performing or faster machine would have motivated one of ordinary skill in the art to modify the design of Damouny to use multiple PLA's for evaluating unique instruction types as taught by Thoma. With

this methodology in place in the disclosure of Damouny, multiple PLA's would be used in place of the single branch PLA so that a PLA that is too large is avoided and no performance degradation occurs.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Damouny to use multiple PLA's, as taught by Thoma, in place of the single branch PLA so that increased speed in the processing machine may be realized.

11. In regard to claim 2, Damouny in view of Thoma discloses the microprocessor according to claim 1, wherein each of the embedded logic circuits includes:

a. a table for performing a table lookup in response to a received instruction; A PLA inherently uses a table. Hennessy (Computer Architecture) explicitly shows on pages 205-206 that a PLA is a table with entries for lookup. In addition, Hennessy (Computer Organization and Design) has shown on pages B-11 to B-13 that a PLA includes a pair of tables, an AND plane and an OR plane. These tables are used to perform table lookups because the inputs into the AND table are transformed into intermediate values that fall down to the OR table and get further transformed into what results as the outputs.

b. and a controller responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup for controllably setting each of the control signals required by the microprocessor for executing said received instruction. As shown in figure 1A, the branch PLA's 180 are responsive to the control variable (element 184), the control signals for an

immediately preceding instruction (element 182), and to the table lookup for setting the required control signals (element 183). The tables use the control signals input to lookup the control signals to be output to element 156 via line 183.

12. In regard to claim 3, Damouny discloses the microprocessor of claim 2, wherein the controller includes:

a. means for setting a control signal to a "1" regardless of its immediately preceding value;

b. means for setting a control signal to a "0" regardless of its immediately preceding value;

c. and means for not modifying a control signal from its immediately preceding value.

Column 3, lines 14-17 show that the control signals are set to active high ("1") and active low ("0"). Since limitations (a) and (b) of the claim state that this setting is regardless of the preceding value, the value may or may not be set based on the previous value and this portion of the limitations is not given weight and these two limitations are met. When the control signal of mention does not change from one instance to the next, the control signal is set to the same value as before and is not modified *from the previous value*, but is modified in general.

13. In regard to claim 4, Damouny discloses the microprocessor of claim 3, wherein the controller further includes: means for setting a control signal to a data state. As

shown above, the control signals are set to active low or active high, a "0" or a "1" respectively. Since a "1" or "0" bit is data, the control is set to a data state.

14. In regard to claim 6, Damouny discloses the microprocessor according to claim 1, further comprising means for determining which of the control signals are not to be modified for each instruction. Since the disclosure of Damouny is of a standard architecture where the control signals are set for each operation, every control signal is modified for each instruction, though some are modified at times to be the same value as a preceding signal. Thus it is determined that none of the control signals are to be not modified, since each signal is set.

15. In regard to claim 9,

a. Damouny discloses a microcode unit in a microprocessor (figure 1A, element 54) for outputting control signals (element 182), for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:

i. an instruction address input for receiving an instruction address; Figure 1A shows that element 156 (and thus the microcode unit) receives addresses on an input via line 168, which is output by element 164, for the next microaddress or microinstruction address.

ii. a control variable input for receiving a control variable corresponding to a current state of the microprocessor; Figure 1A shows that the microcode unite has a control variable input 184. Column 4, lines

57-61 show that the input signals received on bus 184 correspond to and control the internal state.

iii. a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; Figure 1A shows that element 180 (and thus the microcode unit) receives on an input the control signal 182, which is output by element 164 and thus the microcode unit. Column 4, lines 57-61 show that this signal 182 is a control signal. Column 18, lines 1-8 show that the signal on bus 182 is generated in previous instructions and supplied in a next cycle.

iv. And an embedded logic circuit dedicated for evaluating types of instructions received by the microcode unit. Figure 1A shows a PLA element 150 that maps instructions or decodes opcodes. Column 4, lines 33-35 show that this mapping generates pointers necessary for execution and address calculation and thus the instructions are evaluated to generate these pointers. Column 3, lines 41-439 show that this one unit maps or evaluates for each instruction given in appendix B.

b. Damouny does not disclose a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit.

c. Thoma has disclosed in figure 1 the use of multiple PLA embedded logic circuits. The summary shows that the PLA's decode the opcodes of instructions.

Column 2, lines 6-9 show that each PLA is optimized for decoding a given instruction class (or evaluating a unique instruction type).

d. The background section of Thoma shows that prior art PLA decoding using only one PLA results in physically large design and performance degradation manifest in slower machine speeds. The summary shows that the improvement is in using multiple PLA's and thus this performance degradation is avoided. This ability to have a better performing or faster machine would have motivated one of ordinary skill in the art to modify the design of Damouny to use multiple PLA's for opcode decoding as taught by Thoma.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Damouny to include multiple PLA's as taught by Thoma so that increased speed in the processing machine may be realized.

***Conclusion***

16. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references have been cited to further show the art with respect to PLA's and microcode units in general.

"Computer Organization and Design" by Hennessy and Patterson shows that a PLA is constructed as tables for lookup.

"Computer Architecture" by Hennessy and Patterson also shows that a PLA is constructed as tables for lookup.

US Pat No 4,472,772 to Flora teaches a microinstruction execution and control apparatus that uses conditions and signals from previous instructions for control.

US Pat No 4,887,203 to MacGregor discloses microcode control with multiple decoding mechanisms and feedback signals.

US Pat No 5,101,344 to Bonet gives microcode control that is based on previous conditions and external control signals.

US Pat No 5,046,040 to Miyoshi teaches a microprogram control apparatus that uses previous control signals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
April 13, 2004

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